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(54) [Title] CLOCK REPRODUCING CIRCUIT

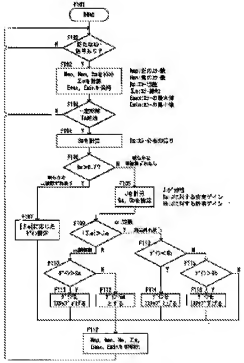
(57) Abstract

Problem

When jitter occurs in the input signal in a clock reproducing circuit that obtains a reproduced clock synchronized with the encoder side based on time reference information transmitted along with the data, the reproduced clock will be unstable.

Means to solve

Whether the input signal and the reproduced clock are synchronized is determined based on the relationship between the absolute value of the total Σe of an error signal output in a prescribed period Ta and jitter width J (F109). When they are synchronized, the gain is changed using stable gain Ga for jitter width J as the target value. When they are not synchronized, the gain is changed using permissible gain Gb for jitter width J as the target value.



[Figure 2 is translated at the end of the document]

Claims

1. A clock reproducing circuit, which is a clock reproducing circuit that generates a reproduced clock synchronized with the data generating side, based on time reference information transmitted along with the aforementioned data,

that is characterized by being provided with an error signal generating means that generates an error signal based on the aforementioned reproduced clock and the aforementioned time reference information in the input data,

a variable gain means that can give a variable amount of gain to the aforementioned error signal,

a gain setting means that sets the gain value in the aforementioned variable gain means based on multiple error signals from the aforementioned error signal generating means,

and a clock generating means that generates the aforementioned reproduced clock based on the error signal output by the aforementioned variable gain means,

and that is characterized in that the aforementioned gain setting means determines whether there is a distinct frequency drift between the frequency of the aforementioned reproduced clock and the frequency of the aforementioned data generating side based on the distribution situation of the aforementioned multiple error signals, and changes the gain in the aforementioned variable gain means according to the determined result.

2. The clock reproducing circuit described in Claim 1, characterized in that the aforementioned gain setting means changes the gain in the aforementioned variable gain means according to the jitter width in the aforementioned multiple error signals when it is determined that there is no distinct frequency drift between the frequency of the aforementioned reproduced clock and the frequency of the aforementioned data generating side.

3. The clock reproducing circuit described in Claim 2, characterized in that when it is determined that there is no distinct frequency drift between the frequency of the aforementioned reproduced clock and the frequency of the aforementioned data generating side, the aforementioned gain setting means determines whether the aforementioned reproduced clock and the aforementioned data generating side are synchronized in the relationship between the total of the aforementioned error signals in a prescribed period and the aforementioned jitter width; when they are synchronized, the gain value is changed toward a first target value that is set based on the aforementioned jitter width, while when they are not synchronized, the gain value is changed toward a second target value that is larger than the aforementioned first target value.

4. The clock reproducing circuit described in Claim 1, characterized in that when it is determined that there is distinct frequency drift between the frequency of the aforementioned reproduced clock and the frequency of the aforementioned data generating side based on the distribution situation of the aforementioned multiple error signals, the aforementioned gain

setting means changes the gain value in the aforementioned variable gain means based on the total of the aforementioned error signals in a prescribed period.

5. The clock reproducing circuit described in Claim 1, characterized in that the aforementioned gain setting means lowers the gain value in the aforementioned variable gain means when it is determined that there is no distinct frequency drift between the frequency of the aforementioned reproduced clock and the frequency of the aforementioned data generating side based on the distribution situation of the aforementioned multiple error signals.

Detailed explanation of the invention

[0001]

Technical field of the invention

The invention is a clock reproducing circuit in a decoder for MPEG2 transport streams (termed "MPEG2-TS" hereafter) in which is included a data storage or digital broadcast receiver, such as a bus-connectible D-VHS (registered trademark), and relates to a clock reproducing circuit that is ideal for devices that receive MPEG2-TS that includes jitter.

[0002]

Prior art

With an MPEG2-TS stream, time reference information called PCR (Program Clock Reference) is inserted at a frequency of one or more times in about 0.1 second. The PCR is generated and added by an MPEG2-TS encoder, and with a decoder that decodes MPEG2-TS, the PCR is referenced, and a system clock synchronized with the system clock of the encoder must be generated in order for video signals or audio signals to be reproduced correctly.

[0003]

One example of such a clock reproducing circuit for MPEG2-TS is shown in Figure 4. In the figure, 1 is a subtracter that outputs error signals based on the PCR value extracted from the MPEG2-TS and the value of the STC (System Time Clock) output from an STC counter 2, 3 is a gain circuit that gives a prescribed gain to the error signals from subtracter 1 and outputs them, and 4 is a digital LPF that applies filter processing to the output from gain circuit 3 and outputs the result.

[0004]

5 is a D/A converter that converts the output from digital LPF 4 to an analog signal and outputs the result, and 6 is a voltage controlled oscillator (VCXO) that outputs a clock with a frequency that changes according to the voltage of the analog signal output from D/A converter 5

using 27 MHz as the center frequency. Then the output from voltage controller oscillator 6 is output to the MPEG2-TS decoder as the system clock as well as being output to STC counter 2, and the STC value output by STC counter 2 is supplied to subtracter 1.

[0005]

Note that when the PCR value received at a certain time is PCR(n) and the STC value at that time is STC(n), and the PCR value received immediately prior is PCR(n-1) and the STC value at that time is STC(n-1), subtracter 1 compares the value of PCR(n-1) subtracted from PCR(n) and the value of STC(n-1) subtracted from STC (n) and outputs the value of the difference between the two values.

[0006]

Here, the PCR value inserted into the MPEG2-TS is a value given by counting a 27 MHz frequency clock in the encoder, and the STC value output by STC counter 2 is a value output from voltage controlled oscillator 6 using 27 MHz as the center frequency. So if the clock frequency in the encoder and the clock frequency from voltage controlled oscillator 6 agree perfectly, an error signal of 0 is output from subtracter 1, but when there is a frequency di8sparity between the two clocks, an error signal corresponding to the magnitude of the disparity is output.

[0007]

A feedback loop is formed by configuring in this way and control is provided so that the same clock as the clock in the encoder is output from voltage controlled oscillator 6.

[0008]

Problems to be solved by the invention

When an MPEG2-TS is received through a bus, however, the MPEG2-TS packet spacing sometimes fluctuates due to transmission clock differences or the transmission format. For this reason, with reception through a transmission route such as a bus, packets will be received with jitter superimposed.

[0009]

Here, when a conventional clock reproducing circuit is used and a TS that includes large jitter is received when the gain in gain circuit 3 is set to be high, the frequency of the system clock output by voltage controller oscillator 6 fluctuates greatly and operation becomes unstable.

[0010]

When a TS that includes jitter is assumed, while the gain is set to be low, fast synchronization cannot be accomplished. Synchronization loss, called drift, also sometimes occurs even after synchronization, and also in this case, fast synchronization cannot be accomplished. When jitter is superimposed on an MPEG2-TS in this way, it is difficult to set the gain setting value for gain circuit 3 at an appropriate value.

[0011]

Means to solve the problems

In order to solve the problems above, the clock reproducing circuit pertaining to the present invention is a clock reproducing circuit that generates a reproduced clock synchronized with the data generating side based on time reference information transmitted along with the aforementioned data. It is characterized by being provided with an error signal generating means that generates an error signal based on the aforementioned reproduced clock and the aforementioned time reference information in the input data, a variable gain means that can give a variable amount of gain to the aforementioned error signal, a gain setting means that sets the gain value in the aforementioned variable gain means based on multiple error signals from the aforementioned error signal generating means, and a clock generating means that generates the aforementioned reproduced clock based on the error signal output by the aforementioned variable gain means, and is characterized in that the aforementioned gain setting means determines whether there is distinct frequency drift between the frequency of the aforementioned reproduced clock and the frequency of the aforementioned data generating side based on the distribution situation of the aforementioned multiple error signals, and changes the gain in the aforementioned variable gain means according to the determined result.

[0012]

The clock reproducing circuit pertaining to the present invention is also characterized in that the aforementioned gain setting means changes the gain in the aforementioned variable gain means according to the jitter width in the aforementioned multiple error signals when it is determined that there is no distinct frequency drift between the frequency of the aforementioned reproduced clock and the frequency of the aforementioned data generating side.

[0013]

The clock reproducing circuit pertaining to the present invention is also characterized in that when it is determined that there is no distinct frequency drift between the frequency of the aforementioned reproduced clock and the frequency of the aforementioned data generating side,

the aforementioned gain setting means determines whether the aforementioned reproduced clock and the aforementioned data generating side are synchronized with respect to the relationship between the total of the aforementioned error signals in a prescribed period and the aforementioned jitter width; when they are synchronized, the gain value is changed toward a first target value that is set based on the aforementioned jitter width, while when they are not synchronized, the gain value is changed toward a second target value that is larger than the aforementioned first target value.

[0014]

The clock reproducing circuit pertaining to the present invention is also characterized in that when it is determined that there is distinct frequency drift between the frequency of the aforementioned reproduced clock and the frequency of the aforementioned data generating side based on the distribution situation of the aforementioned multiple error signals, the aforementioned gain setting means changes the gain value in the aforementioned variable gain means based on the total of the aforementioned error signals in a prescribed period.

[0015]

The clock reproducing circuit pertaining to the present invention is also characterized in that the aforementioned gain setting means lowers the gain value in the aforementioned variable gain means when it is determined that there is no distinct frequency drift between the frequency of the aforementioned reproduced clock and the frequency of the aforementioned data generating side based on the distribution situation of the aforementioned multiple error signals.

[0016]

Embodiment of the invention

The clock reproducing circuit pertaining to the present invention is characterized in that, even when MPEG2-TS that include relatively large jitter are input, the system clock is synchronized with the system clock in the encoder in a short time, while a stable system clock is also obtained with synchronization being completed.

[0017]

Note that the configuration of the clock reproducing circuit pertaining to the present invention is where the configuration for gain setting circuit 7 is added to the clock reproducing circuit shown in Figure 4, as shown in Figure 1. Namely, for the configuration and operation of subtracter 1, STC counter 2, gain circuit 3, digital LPF 4, D/A converter 5 and voltage controlled

oscillator 6, explanations are omitted since they are the same as previously explained, and here, the operation of gain setting circuit 7 is explained.

[0018]

Error signals from subtracter 1 are input to gain setting circuit 7 as shown in Figure 1, and gain setting circuit 7 is configured to set the gain in gain circuit 3 based on the error signals.

[0019]

Figure 2 is a flowchart for explaining the gain setting operation in gain circuit 3 that is set by gain setting circuit 7. In the figure, when an MPEG2-TS is input (F101), first, whether a new error signal has been input is detected (F102). When a new error signal is detected, [processing] advances to Y, and when not detected, the detection operation is repeated until a new error signal is detected.

[0020]

Next, when a new error signal is detected, the number of positive errors Nep, the number of negative errors Nen, the total number of errors Ne, and the error total Σe in the error signals are calculated, while the maximum error value Emax and the minimum error value Emin are also held (F103), and whether a fixed period Ta has been attained after that is detected (F104).

[0021]

Then, when fixed period Ta has been attained, [processing] advances to Y. When fixed period Ta has not been attained, the operation in F102 and F103 is repeated until fixed period Ta is attained.

[0022]

Note that when fixed period Ta in F104 is set to one second here, because the PCR in the MPEG2-TS is input at a frequency of one time per 0.1 second at minimum, in this case, processing will advance to F105 after about ten error signals have been detected in fixed period Ta.

[0023]

At F103, each time a new error is detected, a new number of positive errors Nep, number of negative errors Nen, total number of errors Ne and error total Σe are calculated, while error maximum value Emax and error minimum value Emin are also held, but processing from F105 on is carried out when fixed period Ta has elapsed.

[0024]

Figure 3 shows error signals detected in fixed period Ta. Figure (a) shows when frequency drift between the system clock and the system clock in the encoder is large, and Figure (b) shows when frequency drift is small. Figure (c) shows where large jitter is included where frequency drift is small.

[0025]

Note that with the example shown in Figure (a), the number of positive errors Nep is 9, the number of negative errors Nen is 1, the total number of errors Ne is 10, the error total Σe is 44, the maximum error value Emax is 9, and the minimum error value Emin is -1, for the ten error signals in fixed period Ta. Then error distribution bias Be is calculated as below based on these values (F105).

$Be = |(Nep-Nen)|/Ne$

[0026]

Here, when error distribution bias Be is close to the value 1, it can be determined that drift has clearly occurred between the frequencies of the system clock and the system clock in the encoder. That is, when the error distribution in fixed period Ta is greatly biased either in the positive direction or the negative direction, it can be determined that frequency drift has clearly occurred.

[0027]

Note that with the clock reproducing circuit pertaining to the present invention, using 0.7 as a reference, for example, if the value of error distribution bias Be is a value greater than 0.7, it is determined that distinct frequency drift has occurred (F106), and with a value of 0.7 or less, it is determined that distinct frequency drift has not occurred. That is, with the example shown in Figure 3(a), the value of error distribution bias Be is 0.8, and it is determined that distinct frequency drift has occurred.

[0028]

Then, when it is determined that distinct frequency drift has occurred, the gain is set in gain circuit 3 to a value corresponding to the absolute value of error total Σe (F107). That is, one step, from gain that can be set to multiple steps, is selected and set according to the magnitude of the absolute value of error total Σe. Note that with the example shown in Figure 3(a), the value of error total Σe is 44, so the setting is to a gain at a step corresponding to that value.

[0029]

On the other hand, when the value of error distribution bias Be is a value of 0.7 or less at F106, the jitter width J is next calculated, while the stable gain Ga for jitter width J and the permissible gain Gb for jitter width J are also set (F108). That is, in the case of the error distribution as shown in Figure 3(b), because the value of error distribution bias Be is 0.2, it is determined that distinct frequency drift has not occurred, but there are cases when large jitter is included even when frequency drift has not occurred. Therefore, the gain must be set according to the jitter width.

[0030]

Here, when the gain at which a stable clock can be obtained for a certain jitter width J is found experimentally, it can be seen that if the jitter width is doubled, the stable gain is halved. That is, stable gain Ga for jitter width J is inversely proportional to jitter width J, so the situation will be as below.

$Ga = a/J$ (a is a constant)

[0031]

In addition, when a gain that is permissible so that the clock will not fluctuate too greatly for a certain jitter width J is found experimentally, it can be seen to be inversely proportional to jitter width J in the same way, so the situation will be as below.

$Gb = b/J$ (b is a constant)

[0032]

Stable gain Ga and permissible gain Gb can be set by determining constants a and b as above by experiment or calculation in advance, but in contrast to stable gain Ga that is a gain at which a stable clock can be obtained, permissible gain Gb is a gain that is permissible so that the clock does not fluctuate too greatly, and so the relationship between stable gain Ga and permissible gain Gb is as below.

$Ga < Gb$

Note that these values can also be stored in advance in the device.

[0033]

Next, synchronization loss is detected by comparing a threshold value that is proportional to jitter width J and the absolute value of error total Σe. That is, when the absolute value of error total Σe exceeds the value $J\alpha$ of jitter width J multiplied by a prescribed constant α as shown, it is

judged to be a state of synchronization loss, while when it is less than or equal to the value $J\alpha$ of jitter width J multiplied by a prescribed constant α, it is judged to be a state in which synchronization is achieved (F109).

[0034]

In this way, with the clock reproducing circuit pertaining to the present invention, when jitter width J is a large value, a state in which synchronization is achieved is judged, even when the absolute value of error total Σe is relatively large. This is because when large natural jitter occurs, the absolute value of error total Σe has a tendency to be a large value, and judging the presence of synchronization loss due to the effect of the large jitter, even in a synchronized state, is prevented.

[0035]

Here, Figure 3(c) shows a state in which large natural jitter occurs while synchronization is achieved. When large natural jitter occurs in this way, the absolute value of error total Σe will be a large value due to the influence of the jitter, but with the clock reproducing circuit pertaining to the present invention, this state is judged as a synchronized state, and unnecessary gain fluctuation is avoided.

[0036]

In addition, to counter such naturally occurring large jitter, whether or not there is a synchronized state could also be determined by calculating the total error over a longer period than fixed period Ta by using not only error total Σe in fixed time Ta, but the value of multiple error totals prior to that.

[0037]

Next, when it is determined that synchronization has been achieved, the current gain setting value and stable gain Ga for jitter width J are compared (F110). When the current gain setting value exceeds stable gain Ga, the current gain setting value is lowered one step (F111), and when the current gain setting value is stable gain value Ga or less, the current gain is set as stable gain Ga. In this way, while synchronization is achieved, the gain is changed in a direction so that the current gain setting value is brought closer to stable gain Ga for jitter width J.

[0038]

On the other hand, when it is determined that there is a state of synchronization loss, the current gain setting value and permissible gain Gb for jitter width J are compared (F113), and

when the current gain setting value is less than permissible gain Gb, the current gain setting value is raised one step (F114).

[0039]

In addition, when the current gain setting value is at or above permissible gain Gb, the current gain setting value is additionally compared with permissible gain Gb (F115). When the current gain setting value exceeds permissible gain Gb, the current gain setting value is lowered one step (F116). When the current gain setting value is at or below permissible gain Gb, that is, when the current gain setting value is the same as permissible gain Gb, the gain is not changed. That is, in a synchronized state, gain is changed in a direction so that the current gain setting value will come closer to permissible gain Gb for jitter width J.

[0040]

After gain control as above is carried out, the number of positive errors Nep, the number of negative errors Nen, the total number of errors Ne, the error total Σe, the maximum error value Emax, and the minimum error value Emin are initialized (F117), and detection of a new error signal at F102 is started.

[0041]

In this way, with the clock reproducing circuit pertaining to the present invention, whether or not there is synchronization in the relationship between jitter width J and the absolute value of the error total is determined, and in either state, the gain is changed to a suitable target value corresponding to jitter width J. So even when large jitter occurs in an input MPEG2-TS, the gain in gain circuit 3 can be set to an appropriate value.

[0042]

Then, after the values of the error signals are adjusted with a gain that is set in this way, the analog signal that has passed through digital LPF 4 and D/A converter 5 is supplied to voltage controlled oscillator 6, and a clock that is synchronized with the system clock in the encoder can be obtained quickly.

[0043]

Note that with the application example above, an example was illustrated in which the gain is set according to the jitter width when it is determined at F106 in Figure 2 that distinct synchronization loss has not occurred, but this invention is not limited to this. Control could also be provided to simply lower the gain one step when it is determined that distinct synchronization

loss has not occurred, that is, when the value of error distribution bias Be is 0.7 or less at F106. It will be possible to set the appropriate gain for jitter to a certain extent even with such control, and calculation processing can be reduced.

[0044]

In addition, it goes without saying that it makes no difference whether the configuration for carrying out the gain setting processing above is a configuration using hardware or a configuration using software. It also goes without saying that the clock reproducing circuit pertaining to the present invention can be applied to a D-VHS (registered trademark) provided with a bus interface that conforms to IEEE 1394, a set top box or other audio-video equipment, or another connected device.

[0045]

Effect of the invention

With the clock reproducing circuit according to the present invention, the gain is set based on the distribution situation of multiple error signals. So fast synchronization can be accomplished when there is distinct synchronization loss between the frequency of the reproduced clock and the frequency of the data generating side.

[0046]

In addition, because the gain is set according to the jitter width in multiple error signals, even when large jitter occurs in the input data, the gain can be set according to the jitter, and there is the effect that it is possible to obtain a satisfactory reproduced clock even in a state in which jitter occurs.

[0047]

In addition, with the clock reproducing circuit according to the present invention, whether or not the input data and the reproduced clock are synchronized is determined in the relationship between the total of the error signals in a prescribed period period [sic] and the jitter width, so whether or not there is a synchronized state can be accurately determined even when large natural jitter occurs.

[0048]

In addition, when there is a synchronized state, the gain value is changed toward a first target value that is set based on the jitter value, while when there is no synchronized state, the gain value is changed toward a second target value that is set based on the jitter value and that is

larger than the first target value. So fast synchronization and generation of a stable reproduced clock after synchronization are possible.

[0049]

In addition, when it is determined that there is no distinct synchronization loss between the frequency of the reproduced clock and the frequency of the data reproducing [sic; generating] side based on the distribution situation of multiple error signals, setting of an appropriate gain is possible by carrying out processing to lower the gain without carrying out many calculations.

Brief description of the figures

Figure 1 is a figure for explaining the configuration of a clock reproducing circuit pertaining to the present invention.

Figure 2 is a figure for explaining the operation of gain setting circuit 7.

Figure 3 is a figure showing the error signal distribution.

Figure 4 is a figure for explaining the configuration of a conventional clock reproducing circuit.

Explanation of symbols

1 Subtracter
2 STC counter
3 Gain circuit
4 Digital LPF
5 D/A converter
6 Voltage controlled oscillator
7 Gain setting circuit

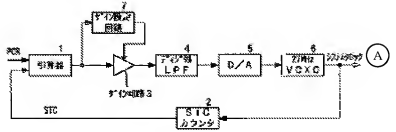


Figure 1

Key: A System clock
1 Subtracter
2 STC counter

3 Gain circuit
4 Digital LPF
7 Gain setting circuit

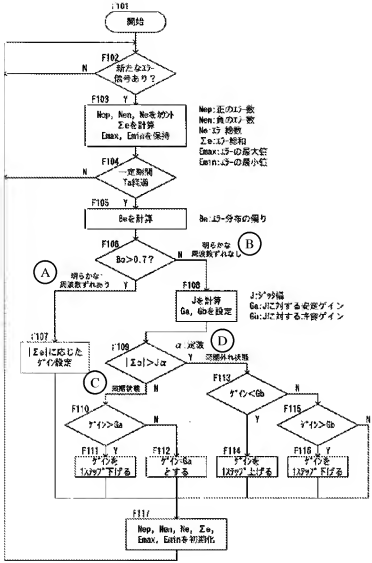


Figure 2

Key: A There is distinct frequency drift
B No distinct frequency drift
C Synchronized
D Synchronization loss
F101 Start
F102 Is there a new error signal?
F103 Nep, Nen, Ne are counted
Σe is calculated
Emax, Emin are held

F104 Fixed time Ta elapsed
F105 Be is calculated
F107 Gain is set according to |Σe|
F108 J is calculated
Ga, Gb are set
F110 Gain > Ga
F111 Gain is lowered one step
F112 Set gain = Ga
F113 Gain < Gb
F114 Gain is raised one step
F115 Gain > Gb
F116 Gain is lowered one step
F117 Nep, Nen, Ne, Σe, Emax, Emin are initialized
Nep: Number of positive errors
Nen: Number of negative errors
Ne: Total number of errors
Σe: Error total
Emax: Maximum error value
Emin: Minimum error value
Be: Error distribution bias
J: Jitter width
Ga: Stable gain for J
Gb: Permissible gain for J
α: Constant

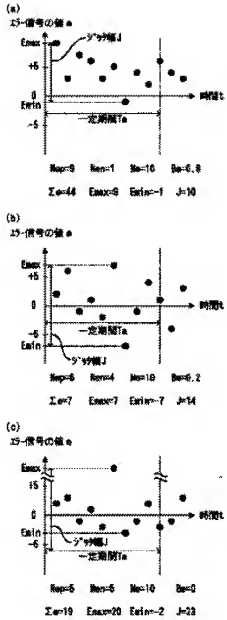


Figure 3

Key: e Error signal value
J Jitter width
t Time
Ta Fixed time

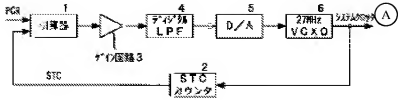


Figure 4

Key: 1 Subtracter
2 STC counter
3 Gain circuit
4 Digital LPF
A System clock

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H 04 L 7/00			7/10	E
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TA00 TC00 TD11 UA05 UA09
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5D044 GK08 GM14 GM15 GM18
5J106 AA04 CC21 CC46 DD13 DD35
EE10 GG07 HH04 KK03 KK25
5K028 AA14 EE03 NN04 NN31
5K047 AA02 AA06 AA12 DD02 GG08
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